TITLE

BI-DIRECTIONAL SHIFT-REGISTER CIRCUIT

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates in general to a shift-register circuit. In particular, the present invention relates to a bi-directional shift-register circuit for driving a liquid crystal display.

Description of the Related Art

A frame of a liquid crystal display (LCD) is generated by a plurality of pixels arranged in an array. Sequential pulses are basic signals for driving the LCD. Sequential pulses are generated by a shift-register circuit, thus, the shift register circuit is a general unit for driving an LCD circuit.

A single scanning turn along one direction, however, does not satisfy all requirements of an LCD product. For example, some digital camera displays are rotated according to the placement angle of the camera. Additionally, some LCD monitors included a monitor rotating function hence LCD displays capable of multiple scanning turns are required. Thus, a shift-register circuit with multiple signal output turns is also required.

In addition, the power consumption of a transmission line is proportional to the amplitude of the signal thereon.

The power loss of the transmission line is obtained as follow:

$$P = fcv^2 \quad ;$$

wherein P is power loss of the transmission line, f is a frequency, c is a parasitic capacitance of the transmission line, and v is the voltage difference of a clock signal.

Therefore, the conventional shift-register circuit requires a relatively high voltage clock supply, which induces high power consumption.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a bi-directional shift-register circuit capable of operating with a low-voltage clock signal supply to reduce power consumption required by clock signal transmission.

According to the above-mentioned objects, the present invention provides a bi-directional shift-register circuit for outputting data in different turns according to a low-voltage clock signal, a first directional signal, and a second directional signal. The bi-directional shift-register circuit comprises a plurality of shift-register units coupled to a first bi-directional control circuit. Each shift-register unit has a level shifter and an input, an output terminal and a clock input terminal for receiving the low-voltage clock signal. The first bi-directional control circuit is coupled to the first-stage output terminal, the third-stage output terminal and the first directional signal or

second directional signal, wherein the first bi-directional control circuit outputs the signal of the first-stage output terminal to the second-stage input terminal when the first bi-directional control circuit receives the first directional signal, and outputs the signal of the third-stage output terminal to the second-stage input terminal when the first bi-directional control circuit receives the second directional signal.

In addition, the present invention provides another bi-directional shift-register circuit comprising thin film transistors for outputting data in different turns according to a low-voltage clock signal, a first directional signal, and a second directional signal. The bi-directional shift-register circuit comprises a plurality of shift-register units that is coupled to a first bi-directional control circuit. Each of the shift-register units has a level shifter and an input, an output terminal and a clock input terminal for receiving the low-voltage clock signal. The first bi-directional control circuit is coupled to the first-stage output terminal, the third-stage output terminal and the first directional signal or second directional signal, wherein the first bi-directional control circuit outputs the signal of the first-stage output terminal to the second-stage first input terminal and outputs the signal of the third-stage output terminal to the second-stage second input terminal when the first bi-directional control circuit receives the first directional signal, and outputs the signal of the third-stage output terminal to the second-stage first input terminal and outputs the

signal of the first-stage output terminal to the second-stage second input terminal when the first bi-directional control circuit receives the second directional signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description and examples with reference made to the accompanying drawings, wherein:

Fig. 1 shows a block diagram of the bi-directional shift-register circuit according to the first embodiment of the present invention;

Fig. 2a shows a block diagram of the bi-directional control circuit according to the first embodiment of the present invention;

Fig. 2b shows a circuit diagram of the bi-directional control circuit according to the first embodiment of the present invention;

Fig. 3a shows a block diagram of the bi-directional shift-register circuit according to the second embodiment of the present invention;

Fig. 3b shows a block diagram of the bi-directional control circuit according to the second embodiment of the present invention;

Fig. 4 shows the bi-directional shift-register circuit using the level shifters according to the first embodiment of the invention;

Fig. 5 shows the circuit of the level shifter and the bi-directional shift-register circuit of the Fig. 4;

Fig. 6 shows the bi-directional shift-register circuit using the level shifters according to the second embodiment of the invention;

Fig. 7 shows the circuit of the level shifter and the bi-directional shift-register circuit of the Fig. 6;

FIG. 8 is a diagram showing simulated timing of the sequential pulse trains (N-1)OUT_2, (N)OUT_2 and (N+1)OUT_2 according to the first and second embodiment using the level shifters.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 1 shows a block diagram of the bi-directional shift-register circuit according to the first embodiment of the present invention. Only three stages of shift-register units are shown in Fig. 1, and a plurality of shift-register units constitute a shift-register circuit. In the present invention, each shift-register unit has a bi-directional control circuit to switch data output turns and directions of the shift-register units.

In FIG. 1, the input signals of the (N-1)th-stage shift-register unit 12 is the output signal (N-2)OUT of the (N-2)th-stage shift-register unit or the output signal (N)OUT of the (N)th-stage shift-register unit 14 output by the bi-directional control circuit 11. The input signals of the (N)th-stage shift-register unit 14 is the output signal (N-1)OUT of the (N-1)th-stage shift-register unit 12 or the output signal (N+1)OUT of the (N+1)th-stage shift-register unit 16 output by the bi-directional control circuit 13. The input signals of the (N+1)th-stage shift-register unit 16 is the output signal

(N)OUT of the (N)th-stage shift-register unit 14 or the output signal (N+2)OUT of the (N+2)th-stage shift-register unit output by the bi-directional control circuit 15. Each shift-register unit comprises a clock input terminal for receiving a clock signal CLK.

For example, the (N)th-stage shift-register unit 14 receives the output signal (N-1)OUT of the (N-1)th-stage shift-register unit 12 or the output signal (N+1)OUT of the (N+1)th-stage shift-register unit 16 through the bi-directional control circuit 13. The shift-register circuit outputs signals in turns of the (N-1)th-stage shift-register unit, the (N)th-stage shift-register unit and the (N+1)th-stage shift-register unit when the data input terminal IN of the (N)th-stage shift-register unit 14 receives the output signal (N-1)OUT of the (N-1)th-stage shift-register unit 12. Conversely, the shift-register circuit outputs signals in turns of the (N+1)th-stage shift-register unit, the (N)th-stage shift-register unit and the (N-1)th-stage shift-register unit when the data input terminal IN of the (N)th-stage shift-register unit 14 receives the output signal (N+1)OUT of the (N+1)th-stage shift-register unit.

The bi-directional control circuit selectively provides data to the data input terminals of the shift-register unit according to the control signal CTR. The control signal CTR is a first directional signal or second directional signal. The shift-register circuit outputs signal in turns of the (N-1)th-stage shift-register unit, the (N) th-stage shift-register unit, and the (N+1)th-stage shift-register unit when the control

signal CTR is the first directional signal. The shift-register circuit outputs signal in turns of the (N+1)th-stage shift-register unit, the (N) th-stage shift-register unit, and the (N-1)th-stage shift-register unit when the control signal CTR is the second directional signal.

Fig. 2a shows a block diagram of the bi-directional control circuit according to the first embodiment of the present invention. The bi-directional control circuit 13 is described, and the other bi-directional control circuit comprises the same circuit except for the received signals. The bi-directional control circuit comprises a first logic device 21, a controlling device 22 and a second logic device 23. Fig. 2b shows a circuit diagram of the bi-directional control circuit according to the first embodiment of the present invention. The first logic device 21 is a NOR logic gate 211. The second logic device 23 is a NOR logic gate 231. The controlling device 23 comprises two switching devices SW1 and SW2.

The NOR logic gate 211 receives the output signal (N-1)OUT of the (N-1)th-stage shift-register unit 12 and the output signal (N+1)OUT of the (N+1)th-stage shift-register unit 16. The NOR logic gate 211 receives a high voltage level signal output from the (N-1)th-stage shift-register unit 12 and a low voltage level signal output from the (N+1)th-stage shift-register unit 16 when the control signal CTR is the first directional signal. Thus, the switching device SW2 is turned on and the NOR logic device 231 outputs the output signal of the (N-

1)th-stage shift-register unit 12 to the (N)th-stage shift-register unit 14.

The NOR logic gate 211 receives a low voltage level signal output from the (N-1)th-stage shift-register unit 12 and a high voltage level signal output from the (N+1)th-stage shift-register unit 16 when the control signal CTR is the second directional signal. Thus, the switching device SW1 is turned on and the NOR logic device 231 outputs the output signal of the (N+1)th-stage shift-register unit 16 to the (N)th-stage shift-register unit 14.

Fig. 3a shows a circuit of the bi-directional shift-register circuit according to the second embodiment of the present invention. In FIG. 3, the input signals of the (N-1)th-stage shift-register unit 32 are the output signal (N-2)OUT of the (N-2)th-stage shift-register unit and the output signal (N)OUT of the (N)th-stage shift-register unit 34 output by the bi-directional control circuit 31. The input signals of the (N)th-stage shift-register unit 34 are the output signal (N-1)OUT of the (N-1)th-stage shift-register unit 32 and the output signal (N+1)OUT of the (N+1)th-stage shift-register unit 36 output by the bi-directional control circuit 33. The input signals of the (N+1)th-stage shift-register unit 36 are the output signal (N)OUT of the (N)th-stage shift-register unit 34 and the output signal (N+2)OUT of the (N+2)th-stage shift-register unit output by the bi-directional control circuit 35. Each shift-register unit comprises a clock input terminal for receiving a clock signal CLK.

For example, the (N)th-stage shift-register unit 34 receives the output signal (N-1)OUT of the (N-1)th-stage shift-register unit 32 and the output signal (N+1)OUT of the (N+1)th-stage shift-register unit 36 through the bi-directional control circuit 33. The shift-register circuit outputs signal in turns of the (N-1)th-stage shift-register unit, the (N)th-stage shift-register unit and the (N+1)th-stage shift-register unit when the data input terminal IN1 receives the output signal (N-1)OUT of the (N-1)th-stage shift-register unit 32 and the data input terminal IN2 receives the output signal (N+1)OUT of the (N+1)th-stage shift-register unit 36. Conversely, the shift-register circuit outputs signal in turns of the (N+1)th-stage shift-register unit, the (N)th-stage shift-register unit and the (N-1)th-stage shift-register unit when the data input terminal IN1 receives the output signal (N+1)OUT of the (N+1)th-stage shift-register unit 36 and the data input terminal IN2 receives the output signal (N-1)OUT of the (N-1)th-stage shift-register unit 32.

The bi-directional control circuit selectively provides data to the data input terminals of the shift-register unit according to the control signal CTR. The control signal CTR is the first directional signal or second directional signal. The shift-register circuit outputs signal in turns of the (N-1)th-stage shift-register unit, the (N) th-stage shift-register unit, and the (N+1)th-stage shift-register unit when the control signal CTR is the first directional signal. The shift-register circuit outputs signal in turns of the (N+1)th-

stage shift-register unit, the (N) th-stage shift-register unit, and the (N-1)th-stage shift-register unit when the control signal CTR is the second directional signal.

Fig. 3b a shows block diagram of the bi-directional control circuit according to the second embodiment of the present invention. The bi-directional control circuit 33 is described, and the other bi-directional control circuit comprises the same circuit except for the received signals. The bi-directional control circuit comprises two controlling device 331 and 334. The switching devices 332 and 335 are turned on when the controlling devices 331 and 334 receive the first directional signal. Thus, the data input terminal IN1 of the (N)th-stage shift-register unit 34 receives the output signal (N-1)OUT of the (N-1)th-stage shift-register unit 32 and the data input terminal IN2 of the (N)th-stage shift-register unit 34 receives the output signal (N+1)OUT of the (N+1)th-stage shift-register unit 36. The switching device 333 and 336 are turned on when the controlling device 331 and 334 receive the second directional signal. Thus, the data input terminal IN1 of the (N)th-stage shift-register unit 34 receives the output signal (N+1)OUT of the (N+1)th-stage shift-register unit 36 and the data input terminal IN2 of the (N)th-stage shift-register unit 34 receives the output signal (N-1)OUT of the (N-1)th-stage shift-register unit 32.

Fig. 4 shows the bi-directional shift-register circuit using the level shifters according to the first

embodiment of the invention. For the sake of clarity, only three stages are exemplified. The level shifter 41 is coupled to the output signal $(N-1)OUT_1$ of the (N-1)th-stage shift-register unit 12 to amplify the output signal $(N-1)OUT_1$ of the (N-1)th-stage shift-register unit 12 to form an output signal $(N-1)OUT_2$ of the level shifter 41. The level shifter 42 is coupled to the output signal $(N)OUT_1$ of the (N)th-stage shift-register unit 14 to amplify the output signal $(N)OUT_1$ of the (N)th-stage shift-register unit 14 to form a output signal $(N)OUT_2$ of the level shifter 42. The level shifter 43 is coupled to the output signal $(N+1)OUT_1$ of the (N+1)th-stage shift-register unit 16 to amplify the output signal $(N+1)OUT_1$ of the (N+1)th-stage shift-register unit 16 to form an output signal $(N+1)OUT_2$ of the level shifter 43.

The bi-directional control circuit receives the output signal of the level shifter. For example, the bi-directional control circuit 13 receives the output signal $(N-1)OUT_2$ of the level shifter 41 and the output signal $(N+1)OUT_2$ of the level shifter 42.

Fig. 5 shows the circuit of the level shifter and the bi-directional shift-register circuit of the Fig. 4. Fig. 6 shows the bi-directional shift-register circuit using the level shifters according to the second embodiment of the invention. Fig. 7 shows the circuit of the level shifter and the bi-directional shift-register circuit of Fig. 6.

FIG. 8 is a diagram showing simulated timing of the sequential pulse trains $(N-1)OUT_2$, $(N)OUT_2$ and $(N+1)OUT_2$ according to the first and second embodiments of using

the level shifters. In this simulation, the amplitude of the clock signal is 3.3V, so the amplitude of the output signal of the level shifter is 9V.

In conclusion, the present invention provides a bi-directional shift-register circuit. Each stage of the bi-directional shift-register circuit includes a shift-register unit, bi-directional control circuit, and level shifter. The circuit configuration allows the bi-directional shift-register circuit to operate with a low-voltage clock signal thus reducing power consumption in transmission of the clock signal.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.